What is claimed is:

1. A termination circuit for a transmission line, the termination circuit comprising:

an input node receiving an input signal over the transmission line;

a pull-down circuit coupled between the input node and a first reference voltage wherein the pull-down circuit is configured to provide an electrical path between the first reference voltage and the input node responsive to the input signal having a first voltage level; and

a pull-up circuit coupled between the input node and a second reference voltage wherein the pull-up circuit is configured to provide an electrical path between the second reference voltage and the input node responsive to the input signal having a second voltage level, wherein the first reference voltage is less than the second reference voltage and wherein the first voltage level is greater than the second voltage level.

wherein the pull-down circuit maintains the electrical path between the first reference voltage and the input node while the input signal is maintained steady state at the first voltage level;

wherein the pull-up circuit maintains the electrical path between the second reference voltage and the input node while the input signal is maintained steady state at the second voltage level.

2. A termination circuit according to Claim 1 wherein the first voltage level comprises a logic high voltage level and wherein the second voltage level comprises a logic low voltage level.

3. A termination circuit according to Claim 1 wherein the first reference voltage comprises a ground voltage and the second reference voltage comprises a supply voltage.

4. A termination circuit according to Claim 1 wherein:

the pull-down circuit is further configured to block the electrical path between the first reference voltage and the input node responsive to the input signal having the second voltage level; and

the pull-up circuit is further configured to block the electrical current path between the second reference voltage and the input node responsive to the input signal having the first voltage level.

5. A termination circuit according to Claim 4 wherein the pull-down and pull-up circuits are further configured to provide electrical paths between the input node and both of the first and second reference voltages at a same time during a transition of the input signal between the first and second voltage levels.

6. A termination circuit according to Claim 1 wherein the pull-down circuit includes a pull-down resistor and a pull-down transistor coupled in series between the input node and the first reference voltage.

7. A termination circuit according to Claim 6 wherein the pull-down circuit includes a first input resistor connected between the input node and a control electrode of the pull-down transistor.

8. A termination circuit according to Claim 7 wherein the pull-down transistor comprises an NMOS transistor.

9. A termination circuit according to Claim 1 wherein the pull-up circuit includes a pull-up resistor and a pull-up transistor coupled in series between the input node and the second reference voltage.

10. A termination circuit according to Claim 9 wherein the pull-up circuit includes a pull-up input resistor connected between the input node and a control electrode of the pull-up transistor.

11. A termination circuit according to Claim 10 wherein the pull-up transistor comprises a PMOS transistor.

12. A termination circuit according to Claim 1 wherein the pull-down

circuit includes a pull-down resistor and a pull-down transistor coupled in series between the input node and the first reference voltage, and wherein the pull-up circuit includes a pull-up resistor and a pull-up transistor coupled in series between the input node and the second reference voltage.

13. A termination circuit according to Claim 12 wherein the pull-down circuit includes a first input resistor connected between the input node and a control electrode of the pull-down transistor, and wherein the pull-up circuit includes a pull-up resistor and a pull-up transistor coupled in series between the input node and the second reference voltage.

14. A termination circuit according to Claim 13 wherein the pull-down transistor comprises an NMOS transistor, and wherein the pull-up transistor comprises a PMOS transistor.

15. A method of terminating a transmission line, the method comprising:

receiving an input signal at an input node;

providing an electrical path between a first reference voltage and the input node responsive to the input signal having a first voltage level; and

providing an electrical path between a second reference voltage and the input node responsive to the input signal having a second voltage level, wherein the first reference voltage is less than the second reference voltage and wherein the first voltage level is greater than the second voltage level;

maintaining the electrical path between the first reference voltage and the input node while the input signal is maintained steady state at the first voltage level;

maintaining the electrical path between the second reference voltage and the input node while the input signal is maintained steady state at the second voltage level.

16. A method according to Claim 15 wherein the first voltage level comprises a logic high voltage level and wherein the second voltage level

comprises a logic low voltage level.

17. A method according to Claim 15 wherein the first reference voltage comprises a ground voltage and the second reference voltage comprises a supply voltage.

18. A method according to Claim 15 further comprising:

blocking the electrical current path between the first reference voltage and the input node responsive to the input signal having the second voltage level; and

blocking the electrical current path between the second reference voltage and the input node responsive to the input signal having the first voltage level.

19. A method according to Claim 18 further comprising:

providing electrical paths between the input node and both of the first and second reference voltages at a same time during a transition of the input signal between the first and second voltage levels.

20. A termination circuit which reduces ringing and dynamic current, which occur when an input signal is transmitted through a transmission line, the termination circuit comprising:

a first switching unit which includes a first termination resistor used to form a path for current flow between a first node and a first voltage when a voltage level of the input signal is inverted to a first level; and

a second switching unit which includes a second termination resistor used to form a path for current flow between the first node and a second voltage when the voltage level of the input signal is inverted to a second level,

wherein termination resistance of the first and second switching units are maintained level to a resistance of the transmission line when the voltage level of the input signal is inverted.

21. The termination circuit of claim 20, wherein the first switching unit comprises a first transistor, including a first end connected to the first voltage and a gate receiving the input signal, and the first termination resistor, which is connected between a second end of the first transistor and the first node.

22. The termination circuit of claim 21, wherein the first switching unit further comprises a first resistor, which is used to protect the gate of the first transistor and is positioned between the first node and the gate of the first transistor.

23. The termination circuit of claim 21, wherein the first transistor is an NMOS transistor.

24. The termination circuit of claim 20, wherein the second switching unit comprises a second transistor, including a first end connected to the second voltage and a gate receiving the input signal, and the second termination resistor, which is connected between a second end of the second transistor and the first node.

25. The termination circuit of claim 24, wherein the second switching unit further comprises a second resistor, which is used to protect the gate of the second transistor and is positioned between the first node and the gate of the second transistor.

26. The termination circuit of claim 25, wherein the second transistor is a PMOS transistor.

27. The termination circuit of claim 20, wherein a voltage level of the first voltage is the same as a voltage level of a ground voltage, and a voltage level of the second voltage is the same as a voltage level of a supply voltage.

28. The termination circuit of claim 20, wherein the first level is high and the second level is low.

29. The termination circuit of claim 20, wherein the termination circuit is mounted in a semiconductor chip.

30. A termination circuit which reduces ringing and dynamic current which occur when an input signal is transmitted through a transmission line, the termination circuit comprising:

a first termination unit which includes a first termination resistor allowing impedance matching to be performed by using a ground voltage when a voltage level of the input signal is inverted to high; and

a second termination unit which includes a second termination resistor allowing impedance matching to be performed by using a supply voltage when a voltage level of the input signal is inverted to low,

wherein termination resistance of the first and second termination units are maintained level to a resistance of the transmission line when the voltage level of the input signal is inverted.

31. The termination circuit of claim 30, wherein the first termination unit further comprises an NMOS transistor, including a first end connected to the ground voltage and a gate receiving the input signal, and the first termination resistor, which is connected between a second end of the NMOS transistor and a first node.

32. The termination circuit of claim 30, wherein the first termination unit further comprises a first resistor, which is used to protect the gate of the NMOS transistor and is positioned between the first node and the gate of the NMOS transistor.

33. The termination circuit of claim 30, wherein the second termination unit further comprises a PMOS transistor, including a first end connected to the supply voltage and a gate receiving the input signal, and

the second termination resistor, which is connected between a second end of the PMOS transistor and the first node.

34. The termination circuit of claim 33, wherein the second termination unit further comprises a second resistor, which is used to protect the gate of the PMOS transistor and is positioned between the first node and the gate of the PMOS transistor.

35. The termination circuit of claim 30, wherein the termination circuit is mounted on a semiconductor chip.

36. A termination circuit which reduces ringing and dynamic current, which occur when an input signal is transmitted through a transmission line, the termination circuit comprising:

a pull-down unit which prevents a voltage level at a first node from reaching a voltage level of a second voltage when a voltage level of the input signal is inverted to a first level; and

a pull-up unit which prevents a voltage level at the first node from reaching a voltage level of a first voltage when a voltage level of the input signal is inverted to a second level.

37. The termination circuit of claim 36, the pull-down unit further comprises:

an NMOS transistor including a first end connected to the first voltage and a gate receiving the input signal; and

a first termination resistor which is connected between a second end of the NMOS transistor and the first node.

38. The termination circuit of claim 37, wherein the pull-down unit further comprises a first resistor, which is used to protect the gate of the NMOS transistor, between the first node and the gate of the NMOS transistor.

39. The termination circuit of claim 36, wherein the pull-up unit further comprises:

a PMOS transistor including a first end connected to the second voltage and a gate to receiving the input signal; and

a second termination resistor which is connected between a second end of the PMOS transistor and the first node.

40. The termination circuit of claim 39, wherein the pull-up unit further comprises a second resistor, which is used to protect the gate of the PMOS transistor, between the first node and the gate of the PMOS transistor.

41. The termination circuit of claim 36, wherein a voltage level of the first voltage is the same as a voltage level of a ground voltage, and a voltage level of the second voltage is the same as a voltage level of a supply voltage.

42. The termination circuit of claim 36, wherein the first level is high, and the second level is low.

43. The termination circuit of claim 36, wherein the termination circuit is mounted in a semiconductor chip.